Bias stress stability of zinc-tin-oxide thin-film transistors with Al_2O_3 gate dielectrics

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The bias stability of zinc-tin-oxide (ZTO) thin-film transistors (TFTs) with either Al_2O_3 gate dielectrics deposited via atomic layer deposition (ALD) or SiO_2 gate dielectrics deposited via plasma-enhanced chemical vapor deposition (PECVD) was compared. Both device types showed incremental mobility ≥ 11 $cm^2/V\,s$, subthreshold slopes <0.4 V/dec, and I_{ON}/I_{OFF} ratios of $\sim 10^7$. During repeated I_D-V_{GS} sweeping, both device types showed positive parallel shift of the turn-on voltage (V_{ON}) without significant degradation of subthreshold slope or mobility, consistent with electron trapping without creation of new traps. A smaller V_{ON} shift was observed in the SiO_2/ZTO devices. In an effort to improve the bias stress stability of the Al_2O_3/ZTO devices, the impact of ALD temperature, plasma exposure of the Al_2O_3, and the addition of an interfacial PECVD SiO_2 capping layer were investigated. The positive bias stress stability of the Al_2O_3/ZTO TFTs was found to be relatively unaffected by the Al_2O_3 ALD temperature, degraded with plasma exposure, and improved by the addition of a thin (~ 3 nm) PECVD SiO_2 interfacial layer between the Al_2O_3 dielectric and the ZTO channel. These results point to the vicinity of the Al_2O_3/ZTO interface as the dominant source of charge trapping. © *2010 American Vacuum Society.* [DOI: 10.1116/1.3455494]

I. INTRODUCTION

Recent reports of thin-film transistors (TFTs) and transparent TFTs based on ZnO (Refs. 1–4) and amorphous oxide semiconductor (AOS) channel materials such as InGaZnO (IGZO) and ZnSnO (ZTO) have generated interest for active matrix organic light emitting diode (AMOLED) display applications.[5–14] Because AMOLED displays are emissive and current driven, high mobility is important and the stability of the TFT current drivers is critical for high visual quality, as shifts in the threshold voltage (V_{th}) during operation will affect pixel brightness. TFT technology is currently dominated by amorphous hydrogenated silicon (*a*-Si:H), yet this material exhibits several drawbacks. Perhaps most significantly, *a*-Si:H mobility is limited to approximately 1 $cm^2/V\,s$. Another major drawback is that significant irreversible instabilities occur during light exposure and bias stressing,[15–17] which must be taken into account when designing circuits, as the devices age during operation.[18] These drawbacks may limit the use of *a*-Si:H in AMOLED display applications.

AOS materials, on the other hand, exhibit mobilities from 5 to >50 $cm^2/V\,s$ even though disordered. This has been explained by the fact that conduction in these materials is through symmetric metal *ns* orbitals, rather than directed covalent sp^3 orbitals.[1] It has been proposed that this bonding arrangement may make AOS materials inherently more stable than *a*-Si:H.[19] ZTO is a promising AOS that has a relatively high mobility of >10 $cm^2/V\,s$ at low processing temperatures.[5,6,14,20–22] Before it can be considered as a replacement for *a*-Si:H as a current driver for AMOLED displays, the operational stability of ZTO-based TFTs must be understood. There have been relatively few studies to date assessing the reliability of ZTO devices. Most reports on ZTO TFTs have used SiO_2 or $AlTiO_x$ (ATO) as the gate dielectric.[14,20,23] In this work, the initial operational stability as well as the long term positive constant voltage stress stability of ZTO TFTs with gate dielectrics consisting of either Al_2O_3 deposited via atomic layer deposition (ALD), SiO_2 deposited via plasma-enhanced chemical vapor deposition (PECVD), or ALD Al_2O_3 capped with a thin layer of PECVD SiO_2 were investigated.

II. EXPERIMENT

A cross-section of the staggered bottom-gate (SBG) TFTs used in this study is shown in Fig. 1. SBG TFTs with width to length $(W/L)=1000/100$ μm were fabricated on indium tin oxide (ITO)-coated glass (Delta Technologies). First, a gate dielectric of either (i) 200 nm Al_2O_3, (ii) 100 nm SiO_2, or (iii) 200 nm Al_2O_3 capped with $\sim 2-5$ nm SiO_2 was blanket deposited on the ITO gate. ALD of Al_2O_3 was performed at 200 °C (unless otherwise noted), using trimethylaluminum (TMA) and water as precursors. SiO_2 was deposited via PECVD at 400 °C using 2% silane (balanced in helium) and nitrous oxide as precursors. Next, using a shadow mask, an approximately 65 nm ZTO channel was deposited via rf sputtering at 5 mTorr working pressure, a 90/10 Ar/O_2 ratio, and, unless otherwise noted, 75 W of rf power. The Zn:Sn ratio is estimated to be roughly 2:1 based on the 2:1 Zn:Sn composition ration of the sputter target. Following the ZTO deposition, devices were annealed in air at 400 °C for 1 h (5 °C/min ramp rate). Finally, ~ 400 nm thick Al contacts were deposited by thermal evaporation and defined using a shadow mask.

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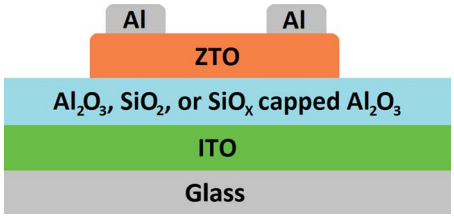

FIG. 1. (Color online) Schematic cross-section of a staggered bottom-gate TFT structure.

Electrical characterization was performed using an Agilent 4155C semiconductor parameter analyzer. Double-sweep I_D-V_{GS} transfer curves were measured with V_{DS} held at +1 V using an integration time of 0.27 s. One double-sweep consisted of ramping V_{GS} from −5 to +20 V and then back to −5 in 0.25 V steps, with a sweep rate of approximately 0.25 V/s. All measurements were made inside a dark box at room temperature in atmosphere. V_{ON} was empirically defined as the onset of drain current in the $\log(I_D)$-V_{GS} transfer curve.[24,25] Subthreshold slope (S) was defined as the maximum slope of $\log(I_D)$-V_{GS} and was reported in units of V/dec of current. Following Hoffman,[25] incremental mobility, μ_{inc}, was extracted from the I_D-V_{GS} curve using

$$\mu_{inc} = (\partial G_d/\partial V_{GS})/(C_{ox}W/L), \quad (1)$$

where G_d is the conductance, C_{ox} is the geometric capacitance of the gate oxide, W is the width, and L is the length of the transistor. The maximum incremental mobility, μ_{inc}(max), is reported. Bias stressing was performed at room temperature in the dark with V_{GS}=+20 V and V_{DS}=+1 V. Stress was interrupted at approximately logarithmic time intervals to measure I_D-V_{GS} transfer curves.

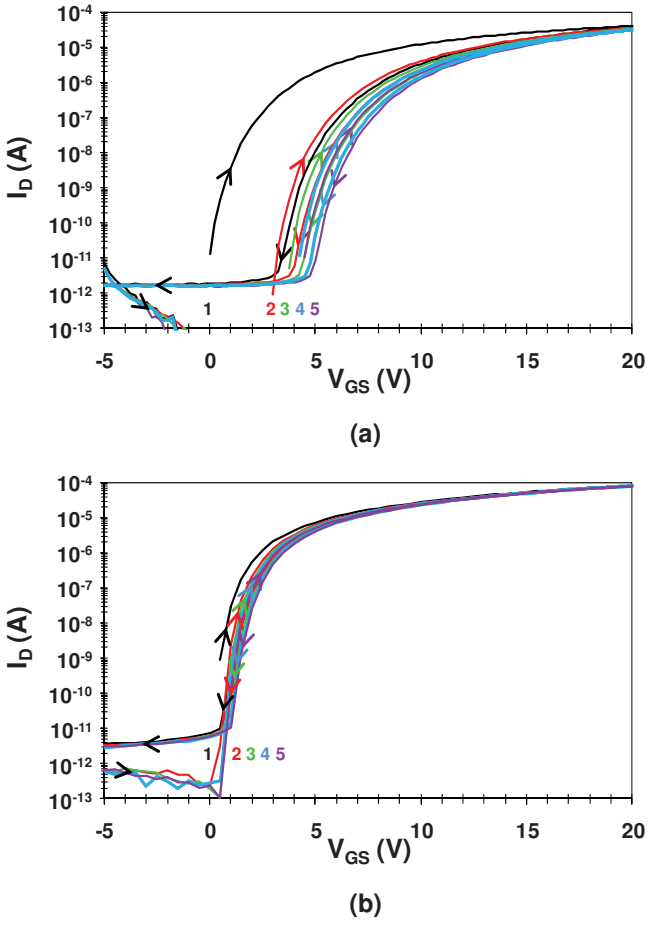

FIG. 2. (Color online) I_D/V_{GS} transfer curves (the initial five sweeps are shown in different colors and numbered sequentially) for ZTO TFTs with either (a) an ALD Al_2O_3 or (b) a PECVD SiO_2 bottom-gate dielectric. The arrows indicate the sweep direction.

III. RESULTS AND DISCUSSION

A. *I-V* and initial behavior

Representative I_D-V_{GS} transfer curves of ZTO TFTs with either (a) a 200 nm Al_2O_3 gate dielectric or (b) a 100 nm PECVD SiO_2 gate dielectric are shown in Fig. 2. The gate capacitance of both device types was roughly equivalent. For both devices, the ZTO channel was deposited at 75 W of rf power. The ZTO TFTs with the Al_2O_3 gate dielectric showed S=0.38 V/dec, I_{ON}/I_{OFF}=~10^7, and μ_{inc}(max) =13.3 cm^2/V s. Comparable performance was observed for PECVD SiO_2 gate dielectric devices with S=0.35 V/dec, I_{ON}/I_{OFF}=~10^7, and μ_{inc}(max)=18.3 cm^2/V s. Although the S values for Al_2O_3 dielectric and SiO_2 dielectric TFTs are similar (due to having similar maximum I_D-V_{GS} slopes), the slope of the I_D-V_{GS} curve of the SiO_2 devices remains steep over a wider voltage range than that of the Al_2O_3 devices, resulting in a sharper overall turn-on and suggesting that the overall trap density at the SiO_2/ZTO interface is lower than that of the Al_2O_3/ZTO interface. It is typically observed, but not widely reported, that AOS TFTs require several *I-V* sweeps before operation is stabilized. It can, therefore, be misleading to report only the first V_{GS} sweep. To give a realistic picture of device operation, the initial set of five sequential double-sweep I_D-V_{GS} curves (V_{GS} swept from −5 to +20 V and then back to −5 V) is shown for each device. For both Al_2O_3 and SiO_2 gate dielectric devices, a positive V_{ON} shift is observed during the initial double-sweeps. By the fifth double-sweep, the large initial clockwise hysteresis has stabilized at approximately 0.30 V for the SiO_2 devices and 0.50 V for the Al_2O_3 devices. In both cases, the curves are shifted roughly parallel, with negligible change in mobility and S, suggesting that the shift is due primarily to charge trapping. The PECVD SiO_2 devices exhibit much less shift; ΔV_{ON} is less than 0.5 V in the first five sweeps compared to a ΔV_{ON} of approximately 4.5 V for the Al_2O_3 devices. Upon the removal of bias, complete recovery of V_{ON} is observed within 36 h at room temperature.

The observation of clockwise hysteresis is consistent with trapping and detrapping of electrons in traps near the interface,[26,27] while the positive V_{ON} shift suggests trapping of electrons further from the interface. The parallel nature of the shift (no significant change in S or mobility) combined with room temperature recovery of V_{ON} after stressing suggests that defect creation is not occurring.[20,28] Since the only difference between the PECVD SiO_2 and ALD Al_2O_3 de-

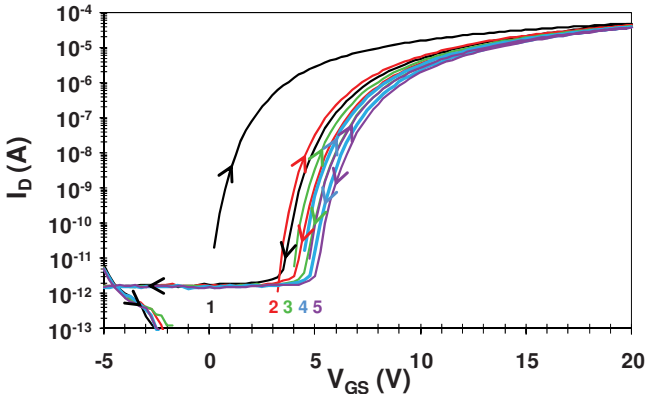

FIG. 3. (Color online) I_D/V_{GS} transfer curves (the initial five sweeps are shown in different colors and numbered sequentially) of ZTO TFTs with ALD Al_2O_3 deposited at 300 °C. The arrows indicate the sweep direction.

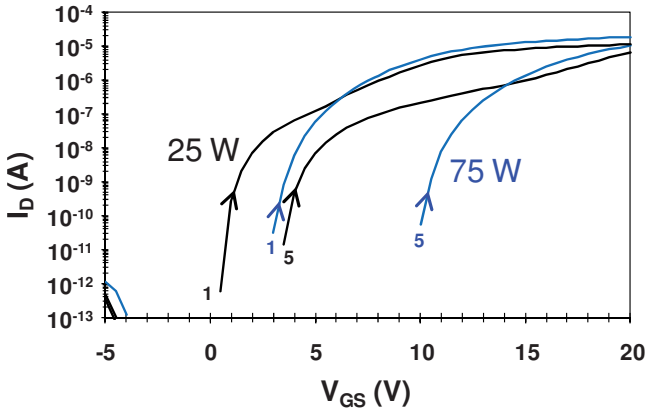

FIG. 4. (Color online) Plot of first and fifth I_D/V_{GS} sweeps for Al_2O_3/ZTO TFTs with the ZTO channel deposited at either 75 W (blue) or 25 W (black) of rf power. The arrows indicate the sweep direction. Only the positive sweep direction is shown.

vices is the gate dielectric, the location of the trapping is suspected to be either at the ZTO/dielectric interface or within the dielectric itself.

Charge trapping-related bias stress instabilities have also been reported in a variety of AOS channel/insulator combinations.[9,20,21,23,26,28,29] Positive bias instabilities in IGZO TFTs with SiO_2 dielectrics have been attributed to traps both in the channel[26] and in the interface/bulk dielectric.[9] Parallel positive transfer curve shifts have been attributed to charge trapping in bulk dielectric defects in ZTO channel TFTs with ALD ATO gate dielectrics[20] and to charge trapping at the channel/dielectric interface in spin coated thermal SiO_2/ZTO TFTs.[21] Gorrn *et al.*[20] reported that the stoichiometry of the ZTO channel deposited via plasma assisted pulsed laser deposition has a large influence on the bias stability of ZTO/ATO TFTs. The ΔV_{ON} of our devices are qualitatively consistent with the reported bias stress behavior of the ZTO TFTs of Gorrn *et al.* with similar stoichiometry (~2:1 Zn:Sn ratio) but different gate dielectric.

There are several other potential process-related causes for the electrical instabilities observed in these bottom-gate TFTs, including the condition of the bottom-gate dielectric surface prior to channel deposition, details of the dielectric deposition process, and plasma damage of the gate dielectric during channel deposition. The underlying substrate can often exert an influence on the crystal structure of an overlying deposited thin film.[30] However, x-ray diffraction (not shown) of ZTO films deposited on both Al_2O_3 and SiO_2 showed the films to be amorphous and unchanged by the underlying material. In an effort to improve bias stress stability of the Al_2O_3 devices and determine the origin of charge trapping, the influence of (i) ALD temperature and (ii) plasma damage of the Al_2O_3 was investigated.

It is known that ALD temperature can have a significant effect on the electrical and physical properties of insulators.[31–33] To investigate the impact of Al_2O_3 ALD temperature on stability, ZTO TFTs were prepared with Al_2O_3 dielectrics deposited at either 200 or 300 °C. The first five double-sweep I_D-V_{GS} transfer curves for a representative 300 °C Al_2O_3 device are shown in Fig. 3 [the 200 °C Al_2O_3 device is shown in Fig. 2(a)]. For the 300 °C device, S = 0.31 V/dec, μ_{inc}(max) = 14.5 $cm^2/V\,s$, and an I_{ON}/I_{OFF} of approximately 10^7 was extracted. In both the 200 and 300 °C devices, a positive parallel V_{ON} shift is observed with each subsequent trace along with a large initial clockwise hysteresis that stabilizes by the fifth sweep at approximately 0.50 V. This close similarity between the two device types indicates that variation of ALD temperature over the range of 200–300 °C does not exert a strong influence on ZTO/Al_2O_3 interface quality, device performance, or device stability.

In SBG TFTs, the gate dielectric is exposed to plasma during rf sputter deposition of the AOS channel (see cross-section in Fig. 1). It is well known that plasma exposure can degrade the electrical properties of gate dielectrics.[34] Oh *et al.*[10] showed that in ZnO-channel bottom-gate TFTs, exposure of the Al_2O_3 dielectric to plasma during rf sputter channel deposition resulted in degradation of the channel/dielectric interface and increased electron-trapping-related bias instabilities. To investigate the effect of plasma exposure on the bias stress stability, ZTO/Al_2O_3 SBG TFTs were fabricated with ZTO sputter deposition performed at two different levels of rf power. Shown in Fig. 4 are the I_D-V_{GS} transfer curves for TFTs with the ZTO channel deposited at either (a) 75 W or (b) 25 W of rf power. Once again, devices were characterized using a sequential series of five double-sweep I_D-V_{GS} transfer curves. For clarity, only the −5 to 25 V positive sweeps for only the first and fifth transfer curves are shown. As expected, when the power was reduced from 75 to 25 W, the positive ΔV_{ON} between the first and fifth gate voltage sweeps was reduced by approximately one-half (from ~7 to ~3 V). The initial V_{ON} shift of the 25 W devices was shifted negatively 25 W compared to that of the 75 W devices (from 3 to 0.5 V). Clockwise hysteresis was slightly reduced from 0.65 to 0.55 V. This result indicates that plasma exposure of the Al_2O_3 during rf sputter deposition of the ZTO channel plays a role in bias instability. However, mobility is degraded, the I_D-V_{GS} response is "kinked," and although ΔV_{ON} is reduced, it is not eliminated in the low

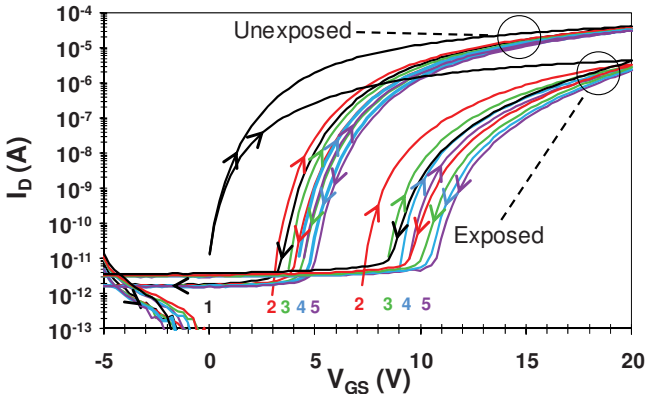

FIG. 5. (Color online) Plot of I_D vs V_{GS} for ZTO TFTs with the bottom Al_2O_3 gate dielectric either left unexposed or exposed to O_2 plasma prior to channel deposition. The initial five sweeps are shown in different colors and numbered sequentially. The arrows indicate the sweep direction.

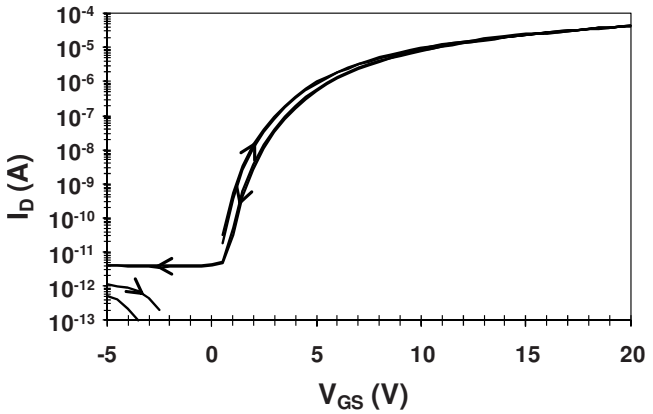

FIG. 6. Plot of I_D vs V_{GS} (the first and fifth double-sweeps are shown) for ZTO TFTs with SiO_2-capped Al_2O_3 gate dielectrics. The arrows indicate the sweep direction.

rf power (25 W) TFTs. Thus, reduced RF power alone is not a viable strategy for improving overall TFT performance.

To further investigate the effect of plasma exposure, TFTs with identical Al_2O_3 dielectrics were exposed to additional O_2 plasma just prior to rf sputtering of the ZTO channel and compared to devices that did not receive the O_2 plasma exposure. The additional O_2 plasma exposure duration was 3 min at 75 W power [20 SCCM (SCCM denotes cubic centimeter per minute at STP) O_2 flow, 20 mTorr pressure]. The initial five double-sweep I_D-V_{GS} transfer curves for the unexposed and O_2 plasma-exposed devices are shown in Fig. 5. The O_2 plasma-exposed devices displayed increased ΔV_{ON} (4.5–10.5 V), degraded mobility, and lower I_{ON}/I_{OFF}, providing further evidence that plasma exposure of the bottom Al_2O_3 dielectric plays a role in the bias instability.

The initial five I_D-V_{GS} sweeps for the ZTO SBG TFTs investigated in this work are characterized by a rigid positive V_{ON} shift. As seen in Fig. 2, ZTO TFTs with PECVD SiO_2 gate dielectrics are more stable than devices with ALD Al_2O_3 gate dielectrics. Because the only difference between the two devices is the bottom-gate dielectric, additional electron trapping either at the Al_2O_3/ZTO interface or in the Al_2O_3 is implicated. Data in Figs. 4 and 5 indicate that plasma exposure of the Al_2O_3 is detrimental. However, the PECVD SiO_2/ZTO interface appears better able to withstand the plasma exposure during channel deposition. In an effort to combine the interface quality of the PECVD SiO_2 with the higher dielectric constant of Al_2O_3, a combination of the two materials was used. The 200 nm ALD Al_2O_3 dielectric was capped with a thin (~2–5 nm) layer of PECVD SiO_2 prior to ZTO channel deposition. The transfer characteristics (for clarity, only first and fifth double V_{GS} sweeps are shown) of this Al_2O_3/SiO_2 "capped"/ZTO device are shown in Fig. 6. Although 0.5 V clockwise hysteresis is still present, the shift in V_{ON} during the initial five I_D-V_{GS} double-sweeps appears negligible. The device parameters of the Al_2O_3/SiO_2 "cap"/ZTO devices are similar to uncapped Al_2O_3 devices: S = 0.46 V/dec, $I_{ON}/I_{OFF} = \sim 10^7$, and μ_{inc}(max) = 12.2 cm^2/V s. The fact that the thin SiO_2 capping layer effectively suppresses V_{ON} shift during initial transfer curve measurements strongly suggests that electron trapping at or very near the channel/Al_2O_3 interface dominates.

B. Bias stressing

To further investigate the source of the V_{ON} instability, ZTO TFTs with ALD Al_2O_3, PECVD SiO_2, and PECVD SiO_2-capped Al_2O_3 gate dielectrics were subjected to extend positive bias stressing. Bias stressing was performed in the dark at room temperature in atmosphere with V_{GS}=+20 V and V_{DS}=+1 V, with stress interrupted at approximately logarithmic time intervals to measure I_D-V_{GS} transfer curves. ΔV_{ON} is defined as the cumulative change in V_{ON} between the initial (unstressed) transfer curve and poststress transfer curve. Analysis of ΔV_{ON} versus time is performed using trapping models. A semilog plot of ΔV_{ON} versus stress time for SBG ZTO TFTs with either ALD Al_2O_3, PECVD SiO_2, or PECVD SiO_2-capped Al_2O_3 gate dielectrics is shown in Fig. 7. For all devices, ΔV_{ON} is positive. Upon the removal of the bias voltage, full V_{ON} recovery was observed after 36 h in the dark at room temperature. For the Al_2O_3 dielectric devices, ΔV_{ON} exhibits a clear logarithmic dependence on stress time,

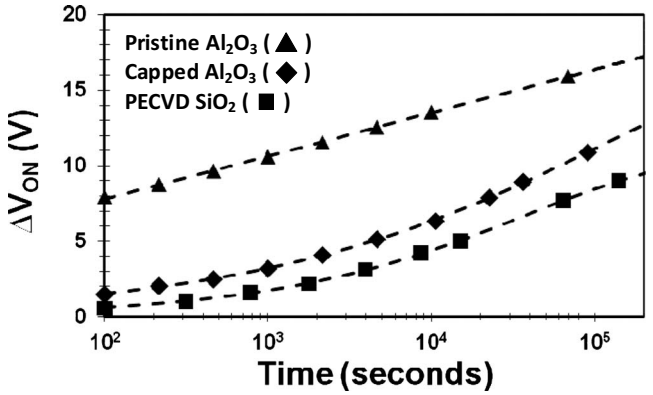

FIG. 7. Semilog plot of ΔV_{ON} vs stress time for ZTO TFTs with either ALD Al_2O_3, PECVD SiO_2, or SiO_2-capped Al_2O_3 gate dielectrics. The dashed lines show the model fits.

indicative of trapping at pre-existing defects with a single capture cross-section, without creation of new defects.[35]

In contrast with the Al_2O_3/ZTO devices, positive bias stressing of the SiO_2/ZTO devices showed a smaller ΔV_{ON} over the 10^5 s time period and exhibited a nonlogarithmic dependence on stress time. Instead, ΔV_{ON} for these devices can be well described by the stretched-exponential model that was originally developed to model bias instabilities in *a*-Si:H,[36] and later used to model trapping in high dielectric constant oxides[37] defined by

$$\Delta V_{ON} = \Delta V_{ON0}\{1 - \exp[-(t/\tau)^{\beta}]\}, \quad (2)$$

where β is the stretching exponent, τ is the characteristic time constant for trap redistribution, and ΔV_{ON0} is the saturation voltage shift, which is asymptotically approached at very long stress times. (Note that since the transfer curves shift rigidly with bias stress, ΔV_{ON} can be substituted for ΔV_{th} in the original formulation of the stretched-exponential model.) For the PECVD SiO_2 dielectric devices, a fit to Eq. (2) yields $\beta=0.47$, $\tau=3.9\times10^5$ s, and $V_{ON0}=10.7$ V.

Similar to the PECVD SiO_2 devices, ΔV_{ON} for the SiO_2-capped Al_2O_3/ZTO TFTs also shows a nonlogarithmic dependence on stress time that can be modeled well by a stretched-exponential time dependence. In this case, fitting ΔV_{ON} to Eq. (2) yields $\beta=0.34$, $\tau=1.2\times10^5$, and $V_{ON0}=18.4$. It is apparent from Fig. 7 that the SiO_2 capping layer not only increases stability but also strongly influences the trapping behavior, with the SiO_2-capped Al_2O_3 gate dielectric devices more closely resembling PECVD SiO_2 devices rather than the Al_2O_3 devices. The similarity between the SiO_2 and the SiO_2-capped devices further suggests that the near-interfacial area dominates trapping in these ZTO devices. Based on the lower magnitude of ΔV_{ON} in SiO_2 and SiO_2-capped TFTs, the trap density is inferred to be lower than that of Al_2O_3.

As developed for *a*-Si:H TFTs,[36] the stretched-exponential model assumes that there is negligible stress-induced defect creation in the channel or at the interface. Libsch and Kanicki[36] interpreted the exponent term, β, to relate to the energy barrier to charge redistribution—the movement of charge at long stress times from shallow to deeper traps. Zafar *et al.*[37] developed a model for charge trapping in metal/oxide/semiconductor (MOS) devices with high-*k* dielectrics which results in the same stretched-exponential equation, but in this case β is interpreted to relate to the width of the distribution of the electron trap capture cross sections. The stretched-exponential equation has been also used to model trapping in several AOS device structures.[9,11,12] Lee *et al.*[12] investigated rf sputtered IGZO TFTs with ALD Al_2O_3 dielectrics with or without a SiN_X capping layer. In interesting contrast to our devices, their TFTs with *uncapped* dielectrics were found to be modeled well by the stretched-exponential equation. Conversely, when the TFT dielectric was capped with SiN_X, the bias stability worsened and ΔV_{ON} became logarithmic with time. It was concluded that the Al_2O_3 dielectric allowed a redistribution of trapped electrons—hence the fit to the stretched-exponential equation—while the capping layer restricted redistribution but had a higher interface trap density.

In this work, the time dependence of the positive bias stress-induced V_{ON} shift is logarithmic for the Al_2O_3/ZTO devices, suggesting trapping at pre-existing defects with a single capture cross-section without creation of new defects. The fact that the addition of a thin interfacial capping layer of PECVD SiO_2 between the Al_2O_3 and the ZTO channel dramatically changes the time dependence of the V_{ON} shift is a strong indication that the interface dominates the positive bias stress response. The close fit of the stretched-exponential model to the SiO_2/ZTO and Al_2O_3/SiO_2-cap/ZTO devices may be interpreted to point to either (i) a redistribution of the trapped charge to deeper states in the SiO_2 (and in the capped devices, the Al_2O_3 layer) or (ii) the presence of a distribution of trap capture cross sections in PECVD SiO_2 layers. Note, however, that Eq. (2) can be arrived at with very different assumptions about defect behavior.[36,37] Without the benefit of additional information about point defects such as that provided by electron spin resonance,[38,39] attaching a specific physical meaning to β is not straightforward.

IV. CONCLUSION

rf sputtered ZTO channel SBG TFTs were fabricated with either ALD Al_2O_3, PECVD SiO_2, or PECVD SiO_2-capped Al_2O_3 gate dielectrics. The initial operational stability was compared using the first five double I_D-V_{GS} sweeps. All devices exhibited clockwise hysteresis and a parallel positive shift of the transfer curve during these initial five sweeps with little change in *S* or mobility, consistent with electron trapping and detrapping at existing defects with little or no creation of new defects. TFTs with an ALD Al_2O_3 dielectric exhibited greater V_{ON} shift than devices with a PECVD SiO_2 dielectric. Increasing the ALD temperature of Al_2O_3 was found to have little influence on the bias instability. On the other hand, exposure of the Al_2O_3 to O_2 plasma degraded both performance and stability, indicating that plasma damage during channel deposition in these SBG TFTs is an important consideration. Decreasing the rf sputtering power during ZTO deposition reduced V_{ON} shift, but resulted in degraded device properties. Protecting the Al_2O_3 from plasma exposure through the addition of a thin (~3 nm) interfacial capping layer between the Al_2O_3 and the ZTO channel was found to greatly improve device stability.

Constant positive bias stressing revealed a logarithmic time dependence of V_{ON} shift in the Al_2O_3/ZTO devices (indicative of trapping at pre-existing defects with a single small capture cross section[35]) but a stretched-exponential time dependence in the SiO_2/ZTO devices. The stretched-exponential time dependence may be interpreted as either a distribution of capture cross sections[30] or redistribution over time of trapped charge into deeper traps.[29] Both the logarithmic and stretched-exponential models are also consistent with little or no creation of new defects. Addition of a thin (~2–5 nm) layer of PECVD SiO_2 between the Al_2O_3 and ZTO channel was sufficient to reduce trapping and dramati-

cally alter the time dependence of the trapping behavior from logarithmic to stretched exponential. Upon the removal of the bias voltage, full recovery of V_{ON} is observed in all devices after 36 h in the dark at room temperature.

Overall, the observation of positive bias induced rigid positive V_{ON} shifts with a strong dependence on the details of the ZTO/dielectric interface accompanied by little change in S and mobility, and full recovery of V_{ON} at room temperature suggests that the bias stability of these SBG ZTO channel TFTs is dominated by electron trapping at the ZTO/dielectric interface or in the dielectric near the interface without significant creation of new defects. Optimization of the ZTO/dielectric interface will be critical for high performance and stable long-term operation. It is likely that a top gate device structure would improve the performance and stability of ZTO/Al_2O_3 TFTs by avoiding exposure of the dielectric surface to plasma during deposition of the channel.

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[1]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature (London) **432**, 488 (2004).
[2]R. L. Hoffman, B. J. Norris, and J. F. Wager, Appl. Phys. Lett. **82**, 733 (2003).
[3]P. F. Carcia, R. S. McLean, M. H. Reilly, and J. G. Nunes, Appl. Phys. Lett. **82**, 1117 (2003).
[4]S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, J. Appl. Phys. **93**, 1624 (2003).
[5]P. Görrn, F. Ghaffari, T. Riedl, and W. Kowalsky, Solid-State Electron. **53**, 329 (2009).
[6]H.-Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, Appl. Phys. Lett. **86**, 013503 (2005).
[7]J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, Jr., X.-H. Zhang, and B. Kippelen, Appl. Phys. Lett. **94**, 142107 (2009).
[8]P. F. Carcia, R. S. McLean, and M. H. Reilly, Appl. Phys. Lett. **88**, 123509 (2006).
[9]J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, Appl. Phys. Lett. **93**, 093504 (2008).
[10]M. S. Oh, K. Lee, J. H. Song, B. H. Lee, M. M. Sung, D. K. Hwang, and S. Im, J. Electrochem. Soc. **155**, H1009 (2008).
[11]K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. **95**, 013502 (2009).
[12]J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang, and H.-I. Kwon, Appl. Phys. Lett. **94**, 222112 (2009).
[13]S.-H. K. Park *et al.*, ETRI J. **31**, 653 (2009).
[14]K. Song, D. Kim, X.-S. Li, T. Jun, Y. Jeong, and J. Moon, J. Mater. Chem. **19**, 8881 (2009).
[15]M. Powell, C. Vanberkel, and J. Hughes, Appl. Phys. Lett. **54**, 1323 (1989).
[16]H. Kavak and H. Shanks, Solid-State Electron. **49**, 578 (2005).
[17]D. L. Staebler and C. R. Wronski, Appl. Phys. Lett. **31**, 292 (1977).
[18]D. R. Allee *et al.*, IEEE Trans. Electron Devices **56**, 1166 (2009).
[19]J. Robertson, Thin Solid Films **516**, 1419 (2008).
[20]P. Görrn, P. Hölzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, Appl. Phys. Lett. **90**, 063502 (2007).
[21]S.-J. Seo, C. G. Choi, Y. H. Hwang, and B.-S. Bae, J. Phys. D: Appl. Phys. **42**, 035106 (2009).
[22]W. S. Cheong, S. M. Yoon, J. H. Shin, and C. S. Hwang, J. Korean Phys. Soc. **54**, 544 (2009).
[23]Y. Jeong, K. Song, D. Kim, C. Y. Koo, and J. Moon, J. Electrochem. Soc. **156**, H808 (2009).
[24]J. F. Wager, D. A. Keszler, and R. E. Presley, *Transparent Electronics* (Springer, New York, 2008), Chap. 5.
[25]R. Hoffman, J. Appl. Phys. **95**, 5813 (2004).
[26]K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, IEEE Trans. Electron Devices **56**, 1365 (2009).
[27]See, for example, T. R. Oldham, *Ionizing Radiation Effects in MOS Devices* (World Scientific, Singapore, 1999), Chap. 2.
[28]R. Cross and M. De Souza, IEEE Trans. Device Mater. Reliab. **8**, 277 (2008).
[29]J. F. Conley, Jr., "Instabilities in amorphous oxide semiconductor thin film transistors," IEEE Trans. Device Mater. Reliab. (in press).
[30]Y. Gao, S. He, P. Alluri, M. Engelhard, A. S. Lea, J. Finder, B. Melnick, and R. L. Hance, J. Appl. Phys. **87**, 124 (2000).
[31]M.-Y. Li, Y.-Y. Chang, H.-C. Wu, C.-S. Huang, J.-C. Chen, J.-L. Lue, and S.-M. Chang, J. Electrochem. Soc. **154**, H967 (2007).
[32]M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George, Chem. Mater. **16**, 639 (2004).
[33]J. L. van Hemmen, S. B. S. Heil, J. H. Klootwijk, F. Roozeboom, C. J. Hodson, M. C. M. van de Sanden, and W. M. M. Kessels, J. Electrochem. Soc. **154**, G165 (2007).
[34]A. Martin, J. Vac. Sci. Technol. B **27**, 426 (2009).
[35]T. H. Ning and H. N. Yu, J. Appl. Phys. **45**, 5373 (1974).
[36]F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).
[37]S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, J. Appl. Phys. **93**, 9298 (2003).
[38]P. M. Lenahan and J. F. Conley, Jr., J. Vac. Sci. Technol. B **16**, 2134 (1998).
[39]P. M. Lenahan and J. F. Conley, Jr., IEEE Trans. Device Mater. Reliab. **5**, 90 (2005).